Amendments to the Claims

1. (Currently Amended) An integrated circuit ~~device~~ having a plurality of input terminals, comprising:

a plurality of input buffers provided corresponding to the plurality of input terminals;

a plurality of serial to parallel conversion circuits provided corresponding to the plurality of input terminals, each of which converts serial output data of the corresponding input buffer ~~for converting outputs of the input buffers~~ from serial to parallel; and

a plurality of boundary scan registers provided corresponding to the plurality of input terminals, each of which is provided in parallel with the corresponding serial to parallel conversion circuit with respect to an output node of the corresponding input buffer~~, serially connected to constitute a shift register, for inputting and outputting scan-in data or scan-out data, the scan-in data being input to the shift register and the scan-out data being output from the shift register~~,

wherein the plurality of boundary scan registers are serially connected to constitute a shift register for inputting and outputting scan-in or scan-out data, the scan-in data being inputted to the shift register and the scan-out data being outputted from the shift register,

wherein each of the plurality of boundary scan registers selectively receives and holds ~~input an input data including~~ one of [[an]] output data of the corresponding input buffer and the scan-in or scan-out data, and ~~holds the input data,~~

~~and selectively output either the input data or an output from one of the serial to parallel conversion circuits~~

wherein each of the plurality of boundary scan registers further receives parallel output data of the corresponding serial to parallel conversion circuit and selectively outputs one of the received parallel output data and the held data to an internal circuit.

2. (Currently Amended) The integrated circuit ~~device~~ according to claim 1, wherein one of the plurality of boundary scan registers comprises:

a first selector circuit for selectively inputting the serial output data of the corresponding input buffer or the input of the scan-in data or scan-out data; and

a second selector circuit for selectively outputting the held ~~input~~ output data or the output data of the corresponding serial to parallel conversion circuit.

3. (Currently Amended) The integrated circuit ~~device~~ according to claim 2, wherein the serial to parallel conversion circuit has a plurality of outputs, and the second selector circuit is provided corresponding ~~in correspondence~~ to the plurality of outputs of the serial to parallel conversion circuit.

4. (Currently Amended) The integrated circuit ~~device~~ according to claim 1, wherein the input terminals include differential input terminal pairs for inputting

differential inputs, respectively, and one of the plurality of input ~~buffer~~ buffers receives the differential inputs, and outputs an input of the serial to parallel conversion circuit.

5. (Currently Amended) An integrated circuit ~~device~~ having a plurality of output terminals, comprising:

a plurality of parallel to serial conversion circuits provided corresponding to the plurality of output terminals, each of which converts parallel output data of an internal circuit ~~for converting an internal signal~~ from parallel to serial;

a plurality of output buffers ~~which are~~ provided corresponding to the plurality of output terminals, ~~and to which an output of the~~ each of which receives serial output data of the corresponding parallel to serial conversion circuit ~~is supplied~~; and

a plurality of boundary scan registers provided corresponding to the plurality of output terminals, each of which is provided in parallel with the corresponding parallel to serial conversion circuit with respect to an output node of the internal circuit, ~~serially connected to constitute a shift register, for inputting and outputting scan-in data or scan-out data, the scan-in data being input to the shift register and the scan-out data being output from the shift register,~~

wherein the plurality of boundary scan registers are serially connected to constitute a shift register for inputting and outputting scan-in or scan-out data, the scan-in data being inputted to the shift register and the scan-out data being outputted from the shift register,

wherein each of the plurality of boundary scan registers selectively receives and holds one of the output data of the internal circuit,~~input an input data including one of an output of the input buffer~~ and the scan-in or scan-out data, and ~~holds the input data, and selectively output either the input data or an output from one of the serial to parallel conversion circuits~~

wherein each of the plurality of boundary scan registers further receives serial output data of the corresponding output buffer and selectively outputs one of the received serial output data and the held data to the corresponding output terminal.

6. (Currently Amended) The integrated circuit ~~device~~ according to claim 5, wherein one of the plurality of boundary scan registers comprises:

a first selector circuit for selectively inputting the ~~internal signal~~ output data of the internal circuit or the input of the scan-in data or scan-out data; and

a second selector circuit for selectively outputting the held ~~input~~ output data or the output data of the corresponding output buffer.

7. (Currently Amended) The integrated circuit ~~device~~ according to claim 6, wherein the output buffer outputs a differential output, and the second selector circuit selectively outputs a complementary ~~signal~~ output data of the held ~~input~~ output data or the differential output data of the corresponding output buffer.

8. (Currently Amended) The integrated circuit device according to claim 6, wherein a plurality of the ~~internal signals~~ output data are input into the parallel to serial conversion circuit, and an AND signal, an OR signal, or an exclusive OR signal of the plurality of ~~internal signals~~ output data are input to the first selector circuit ~~as the internal signal~~.

9. (Currently Amended) An integrated circuit ~~device~~ having a plurality of output terminals, comprising:

a plurality of parallel to serial conversion circuits provided corresponding to the plurality of output terminals, each of which converts parallel output data of ~~for converting~~ an internal ~~signal~~ circuit from parallel to serial;

a plurality of output buffers ~~which are~~ provided corresponding to the plurality of output terminals~~, and to which an output of one of the parallel to serial conversion circuits is supplied~~; and

a plurality of boundary scan registers provided corresponding to the plurality of output terminals, each of which provided in parallel with the corresponding parallel to serial conversion circuit with respect to an output node of the internal circuit~~, serially connected to constitute a shift register, for inputting and outputting scan-in data or scan-out data, the scan-in data being input to the shift register and the scan-out data being output from the shift register~~,

wherein the plurality of boundary scan registers are serially connected to constitute a shift register for inputting and outputting scan-in or scan-out data, the scan-

in data being inputted the shift register and the scan-out data being outputted from the shift register,

wherein each of the plurality of boundary scan registers selectively receives and holds one of the output data of the internal circuit, ~~input an input data including one of an output of the input buffer~~ and the scan-in or scan-out data, and ~~holds the input data, and selectively output either the input data or an output from one of the serial to parallel conversion circuits~~

wherein each of the plurality of boundary scan registers further receives serial output data of the corresponding parallel to serial conversion circuit and selectively outputs one of the received serial output data and the held data to the corresponding output buffer.

10. (Currently Amended) The integrated circuit ~~device~~ according to claim 9, wherein one of the boundary scan registers comprises:

a first selector circuit for selectively inputting the ~~internal signal~~ output data of the internal circuit or the input of the scan-in data or scan-out data; and

a second selector circuit for selectively outputting the held ~~input~~ output data or the output data of the parallel to serial conversion circuit.